For every multiplexor, I used a 2-bit input to represent the S1 and S0.

I used an extra multiplexor to disable clock when the S1 and S0 are both 0 so that nothing would happen and there would be no shift in this case.

I plugged B\_in into the shift right case of the first multiplexor and the shift left case of the last multiplexor so that this could be the bit shifted in.

Then I connected from the first multiplexor and A7 to the last multiplexor and A0. This part is simply shift register.

I then connected A7 to the shift circular right case of the A6’s multiplexor, A6 to A5’s and so on. But I connected A0 to shift circular right case of the A7’s multiplexor to achieve a circular shift.

At last I used another multiplexor as the next bit of A0 (A-1) if the case is shift right and the previous bit of A7(A8) if the case is shift left. In this way the bit shifted out can be shown as well.